ABSTRACT OF THE DISCLOSURE

Multiprocessor system, having a translation lookaside buffer (TLB) in each processor, and having a structure for avoiding TLB purge overhead. Each processor node is provided with a partial main memory and a physical page map table (PPT). The PPT stores mapping between physical page number of main memory and virtual page number. Every memory access transaction for other node specifies physical address and virtual page number. Instead of strictly maintaining TLB coherency by broadcasting TLB purge transaction, an access destination node checks the coincidence between the virtual page number specified in the memory access transaction and the virtual page number mapped in the PPT when the transaction is received. If both are coincident, the memory access is executed. If not coincident, an error message is transferred to an access requesting source.